Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-9. Canceled

10. (Currently Amended) A device for determining the frame boundaries of serialized framed data, the device comprising:

a serial to parallel converter for converting the serialized framed data to a parallel framed data;

a first register for receiving ~~a second output of~~ the parallel framed data from the serial to parallel converter and outputting a first output data word of the parallel framed data at a current cycle clock;

a second register for receiving [[a]] the first output data word ~~of the parallel framed data from the first register~~, and outputting a second output data word corresponding to a previous first output data word from the first register of a previous cycle clock;

~~a first selector for selecting a portion of the first output of the parallel framed data and a portion of the second output of the parallel framed data to form a data word wherein the data word is a concatenation of the portion of the first and second outputs of the parallel framed data;~~

~~a second selector for selecting a first one of the second output of parallel framed data and the concatenated data word~~;

a selector having a first port coupled to the second output data word, a second port coupled to a shifted data word, and a third port configured to select the second output data word or the shifted data word, wherein the shifted data word is a concatenation of a portion of the first output data word and a portion of the second output data word;

a guesser for guessing a position of a frame boundary in the output data word selected by the ~~second~~ selector;

a rotator for rotating the selected data word in accordance with the position guessed by the guesser;

a third register for storing a ~~delayed~~ previous version of the rotated data word;

a ~~third selector~~ select logic unit for ~~selecting~~ combining a portion of the data word held in the rotator and a portion of data word held in the third register to form a data output block comprising ~~multiple frames of the serialized framed data~~ two or more synchronization patterns;

a fourth register for storing the data output block;

a tester ~~for testing the data output to determine if the frame boundaries are at predetermined positions in the data output~~ coupled to the fourth register for simultaneously monitoring the two or more synchronization patterns in the data output block;

a counting mechanism ~~for counting when a frame boundary is at a predetermined position in the data output and further counting when a frame boundary is not at a predetermined position~~ coupled to the tester and being configured to count the number of valid and invalid synchronization patterns; and

a state machine determining if the device is in a state of synchronization based on the counting mechanism, wherein said state machine ~~further causing the second first selector to select a second one of the second output of parallel framed data and the concatenated data word if the device is determined to not be in a state of synchronization.~~ is coupled to the third port of the selector and selectively provides the second output data word or the shifted data word to the guesser and the rotator.

11. (Previously presented) The device of claim 10 further comprising:

an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser.

12. (Previously presented) The device of claim 11, wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary.

13. (Currently Amended) The device of claim 10 wherein the portion of the first output data word comprises first arriving serial bits of the parallel framed data at the current

cycle clock and the portion of the second output data word comprises bits of the previous first output data word from the first register at the previous cycle clock starting at an offset of an odd number of bits from the first arriving bits. ~~of the parallel framed data comprises bits of the first parallel framed data starting at an offset of an odd number of bits from the first arriving serial bits, and the portion of the second output of the parallel framed data comprises the first arriving odd number of bits from the second parallel framed data~~.

14. (Previously presented) The device of claim 13, wherein the odd number of bits is one.

15. (Previously presented) The device of claim 10, wherein the serialized framed data comprises a plurality of frames, each frame comprising comprises a data field and a synchronization pattern.

16. (Previously presented) The device of claim 15, wherein the data field comprises 64 bits and the synchronization pattern comprises two bits.

17. (Previously presented) The device of claim 10, wherein the serialized framed data is 10 Gb Ethernet data.

18.-20. Canceled.

21. (New) The device of claim 10, wherein the counting mechanism comprises:

a first counter for counting the number of valid synchronization patterns in the data output block; and

a second counter for counting the number of invalid synchronization patterns in the data output block.

22. (New) The device of claim 10, wherein the state machine resets the first and second counters when the state machine determines a change in the state of synchronization.

23. (New) The device of claim 10, wherein the state of synchronization is obtained when the state machine detects a predetermined number of consecutive valid synchronization patterns in the serialized framed data.

24. (New) The device of claim 10, wherein the first and second output data words are an integer multiple of eight (8) bits.

25. (New) The device of claim 10, wherein the width (or length) of the fourth register is greater than the width (or length) of the first, second, or third register.